CLAIMS:

1. A method for synchronising start of cell times in input/output means with cell transmission periods in at least one cross-connection means for packet switching,

- where cells are transferred between said input/output means by said cross-connection means in cell transfer periods,
- where configurations of said cross-connection means are changed between cell transfer periods in cross-connection configuration periods,
- where cells from said input/output means are sent at start of cell times, and
- where said sent cells are received in said cross-connection means,

characterized by

- oscillating said configuration between a loopback configuration and a no-transmission configuration during a set up period,
- whereby received cells are transferred back to said sending input/output means in said loopback configuration and received cells are not transferred back to said sending input/output means in said no-transmission configuration,
- receiving back transferred cells in said input/output means,
- checking said received cells in said input/output means for a transmission error,
- shifting an offset of said start cell times in case a transmission error occurred,
- until transferring back at least one cell is wholly carried out within a cell transfer period.

2. A method according to claim 1, characterized by shifting said offset of start of cell times in said input/output means, respectively, to align the time sent cells from said input/output means are received in said cross-connection means.

3. A method according to claim 1, characterized by controlling said start of cell times, said offset of start of cell times and said cross-connection configuration times by a central clock signal.

4. A method according to claim 1, characterized by calculating start of cell times based on a start of cell signal and said offset of said start of cell times, serialising said cells,

and sending said serialised cells together with said start of cell signal at said start of cell times.

5. A method according to claim 1, characterized by receiving transferred back cells, de-serialising said cells and checking each second cell for transmission errors.

6. A method according to claim 1, characterized by receiving transferred back cells, de-serialising said cells and evaluating a bit error indicator.

7. A method according to claim 3, characterized by shifting said offset of start of cell times using an offset counter and changing said offset counter by an amount of clock cycles of said central clock signal.

8. A method according to claim 1, characterized by shifting said offset of said start of cell times to a maximum without generating transmission errors, and shifting said offset of said start of cell times to a minimum without generating transmission errors.

9. A method according to claim 6, characterized by setting said offset of said start of cell times in between said maximum and said minimum.

10. A packet switch comprising:

- input/output means with a port controller with a cell input port and a cell output port,
- cross-connection means comprising cell input ports and cell output ports connected to said cell output port and cell input port of said port controllers, respectively,

characterized in

- that said port controller comprises:
  - a start of cell signal generator for generating start of cell signals,
  - an offset controller for shifting a start of cell time based on said start of cell signal, and
  - an error detection means for detecting corrupt received cells, and
- that said cross-connection means comprises:
  - a configuration controller for controlling an oscillation between a loopback configuration and a no-transmission configuration of said cross-connection means.

11. A packet switch according to claim 10, characterized in that a central clock generator is provided for providing a central clock signal, and that said start of cell signal generator, said offset controller, and said configuration controller comprise an input port for said central clock signal.

12. A packet switch according to claim 10, characterized in that said port controller comprises a serialiser and a de-serialiser for serialising cells to be sent and de-serialising received cells.

13. A packet switch according to claim 10, characterized in that said cross-connection means comprise a NxN crossbar matrix, selectively connecting N cell input ports with N cell output ports.

14. A packet switch according to claim 13, characterized in that said loopback configuration is realised by a unit matrix and a no-transmission configuration is realised by a null matrix.

15. A packet switch according to claim 10, characterized in that said error detection means is a bit error indicator.

16. Use of a method according to claim 1 or a packet switch according to claim 10 in packet switched networks for synchronising start of cell times in various port controllers during a set up to allow configuration changes in cross-connection means without disturbing cell transfers.